

SHRI VILEPARLE KELAVANI MANDAL’S

**SHRI BHAGUBHAI MAFATLAL POLYTECHNIC**

**COMPUTER ENGINEERING DEPARTMENT**

**ACADEMICS YEAR :- 2023 – 2024 Date:11/3/2023**

**COURSE:- MICROPROCESSOR BASED SYSTEM**

**COURSE CODE :- MBS190806**

**ASSIGNMENT 1**

**---------------------------------------------------------------------------------------------------------**

**Q1 . Draw the PIN diagram of 8086.**

**Q2. Draw and explain each block that is [ EU , BIU] of 8086 architecture with**

**Example (MOV al,01H,ADD al,05H).**

**Q3. Describe the concept of Memory Segmentation of 8086. Draw diagram and show segment address.**

**Q4. Describe the Physical Address Generation step with suitable example.**

**Q5. Describe the Memory bank concept and explain the four cases of**

**memory bank access.**

**Q6. Describe the addressing mode of 8086 with example of each.**

**Q7. What will be the content of AL,BL,AX and Dx register after the execution**

**of following instruction and also write which flag will be effected.**

**Mov al,03H**

**Mov bl,03H**

**SUB al , bl**

**MUL al,08H**

**Q8. Identify the Addressing mode of the following instruction: -**

1. **MOV ds, ax**
2. **MOV al , [4172 H ]**
3. **ADD al,[SI]**
4. **ADD ax , [SI] [BX] [04]**
5. **INC [4172 H]**
6. **STC**
7. **DIV BL**
8. **MOV ax , 50H**
9. **CLD**

**10 ) MOV ax , [BX + SI + 03H]**